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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,394	12/28/2001	Seong-jae Lee	2013p006	8538

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,394	LEE ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7-12 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7-12 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. A new rejection is made as set forth in this Office Action. Claims (1, 4-5, 7-12, and 15-20) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 7-9, 11, 12, and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et al. (U.S. Patent 6,316,319).

In re claim 1, **Ishida** discloses a method of fabricating an integrated circuit comprising: forming a diffusion barrier layer pattern **(4 and 5)** on a semiconductor substrate 1 (col. 3, lines 46-57 and **FIGS. 2 and 3**);

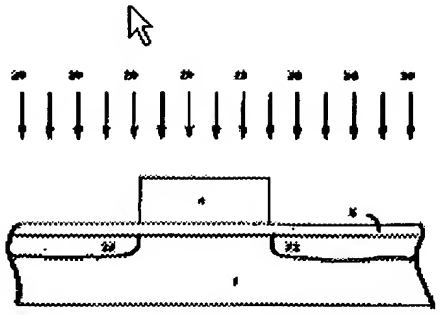

FIG.2

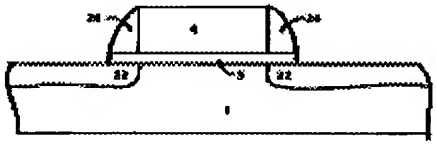

FIG. 3

forming a SOG layer **30** containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements (col. 4, lines 40-64 and **FIG. 5**);

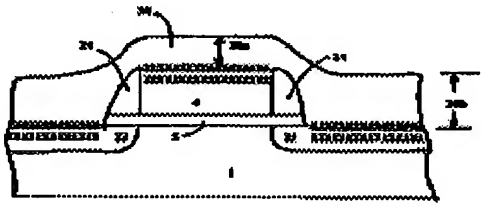

FIG. 5

additionally implanting impurity ions **40** into portions of the SOG layer **30** formed on the diffusion barrier layer **(4 and 5)** and the semiconductor substrate **1**

to increase the concentration of impurities in the SOG layer (col. 5, lines 21-44 and **FIG. 6**); and

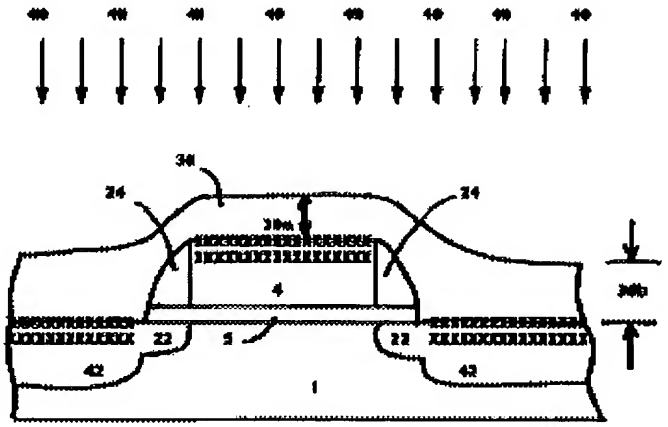

FIG. 6

diffusing the impurity ions contained in the SOG layer having the increased concentration of impurities into the semiconductor substrate by a solid phase diffusion method to form shallow junctions (col. 5, lines 60-65).

In re claim 7, **Ishida** discloses wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing (col. 5, lines 60-65).

In re claim 8, **Ishida** discloses wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of about 900° C to about 1100° C in an inert gas atmosphere (col. 5, lines 60-65).

In re claim 9, **Ishida** discloses wherein in the spike annealing, the semiconductor substrate on which the SOG layer having the increased

concentration of impurities is formed is rapidly thermally annealed at a temperature of about 900° C to about 1100 °C in an inert gas atmosphere (col. 5, lines 60-65).

In re claim 11, **Ishida** discloses a method of fabricating an integrated circuit comprising: forming a gate pattern **4** on a semiconductor substrate **1** (col. 3, lines 46-57 and **FIGS. 2 and 3**); forming a SOG layer **30** containing impurities, including either one of a p-type impurity and an n-type impurity on the entire surface of the semiconductor substrate **1** by spin-coating and densifying a liquid silicate glass including one of P, B, In, As, and Sb doping elements (col. 4, lines 40-64 and **FIG. 5**); additionally implanting impurity ions **40** into portions of the SOG layer **30** formed on the gate pattern **4** and the semiconductor substrate **1** increase the concentration of impurities in the SOG layer (col. 5, lines 21-44 and **FIG. 6**); and diffusing the impurity ions contained in the SOG layer into the semiconductor substrate by a solid phase diffusion method to form shallow junctions having a LDD region self-aligned underneath both sidewalls **24** of the gate pattern **4** and a highly doped source/drain regions adjacent to the LDD region (col. 5, lines 60-65).

In re claim 12, **Ishida** discloses wherein the ratio of the thickness of the SOG layer **30** to the height of a gate electrode **4** constituting the gate pattern is between 1: 1.5 and 1: 10 **(FIG. 6)**.

In re claim 17, **Ishida** discloses wherein the shallow junctions are formed by the solid phase diffusion method using one of rapid thermal annealing (RTA), spike annealing, and laser annealing (col. 5, lines 60-65).

In re claim 18, **Ishida** discloses wherein in the RTA, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of about 900° C to about 1100 °C in an inert gas atmosphere (col. 5, lines 60-65).

In re claim 19, **Ishida** discloses wherein in the spike annealing, the semiconductor substrate on which the SOG layer having the increased concentration of impurities is formed is rapidly thermally annealed at a temperature of about 900° C to about 1100 °C in an inert gas atmosphere (col. 5, lines 60-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 5, 10, 15, 16, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et al. (U.S. Patent 6,316,319) in view of Kroner et al. (IEEE 2000).

In re claim 4 and 15, **Ishida** does not explicitly disclose wherein the concentration of impurities of the SOG layer is increased using a plasma ion implanter including a Plasma Immersion Ion Implanter (PIII) and an Ion Shower Implanter (ISI).

Kroner et al., however, disclose (page 476) wherein the concentration of impurities of a layer is increased by using a plasma ion implanter including an Ion Shower Implanter (ISI) and Plasma Immersion Ion Implanter (PIII). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Ishida and Kroner to enable the process of additionally implanting impurity ions into portions of the SOG layer of Ishida to be formed and furthermore it is a doping method for high dose and low energy implants (page 476, Abstract).

In re claims 5, 10, 16, and 20, **Ishida** discloses wherein the maximum impurity implantation concentration of the SOG layer additionally implanted with the impurity ions is adjusted to $10^{14} - 10^{16}$ cm^{-3} (col. 5, lines 21-36) but does not explicitly disclose the ranges for the maximum impurity implantation concentration, the rapidly thermally annealed temperature of the SOG layer, and the doping depth and doping concentration of the shallow junctions. However, there is no evidence indicating that the ranges for the maximum impurity implantation concentration, the rapidly thermally annealed time duration of the SOG layer, and the doping depth and doping concentration of the shallow junctions is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP§2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable

recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.

W. DAVID COLEMAN
PRIMARY EXAMINER